

Complementary Switch FET Drivers

FEATURES

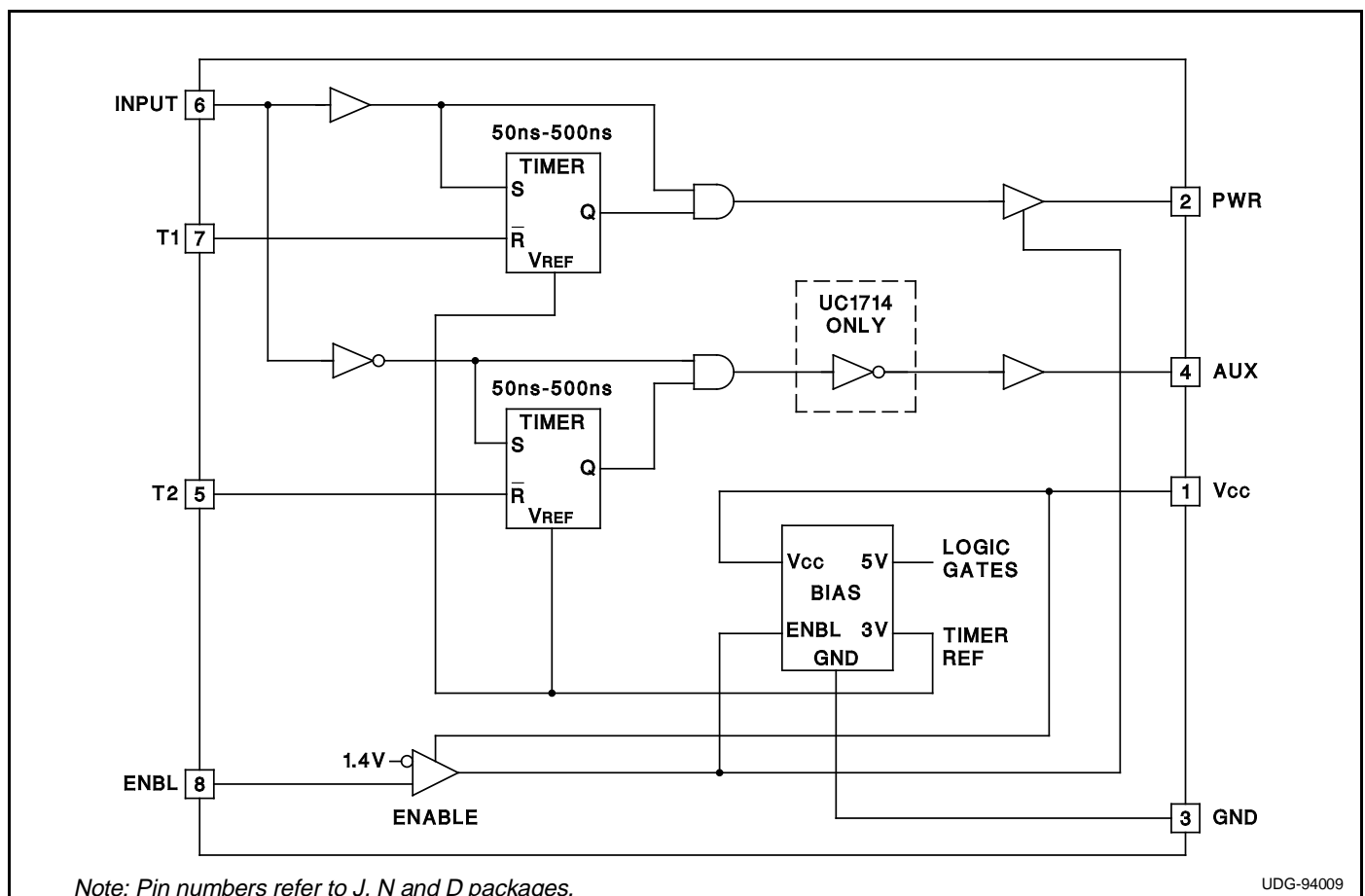
- Single Input (PWM and TTL Compatible)
- High Current Power FET Driver, 1.0A Source/2A Sink
- Auxiliary Output FET Driver, 0.5A Source/1A Sink
- Time Delays Between Power and Auxiliary Outputs Independently Programmable from 50ns to 500ns
- Time Delay or True Zero-Voltage Operation Independently Configurable for Each Output
- Switching Frequency to 1MHz
- Typical 50ns Propagation Delays
- ENBL Pin Activates 220 μ A Sleep Mode
- Power Output is Active Low in Sleep Mode
- Synchronous Rectifier Driver

DESCRIPTION

These two families of high speed drivers are designed to provide drive waveforms for complementary switches. Complementary switch configurations are commonly used in synchronous rectification circuits and active clamp/reset circuits, which can provide zero voltage switching. In order to facilitate the soft switching transitions, independently programmable delays between the two output waveforms are provided on these drivers. The delay pins also have true zero voltage sensing capability which allows immediate activation of the corresponding switch when zero voltage is applied. These devices require a PWM-type input to operate and can be interfaced with commonly available PWM controllers.

In the UC1714 series, the AUX output is inverted to allow driving a p-channel MOSFET. In the UC1715 series, the two outputs are configured in a true complementary fashion.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

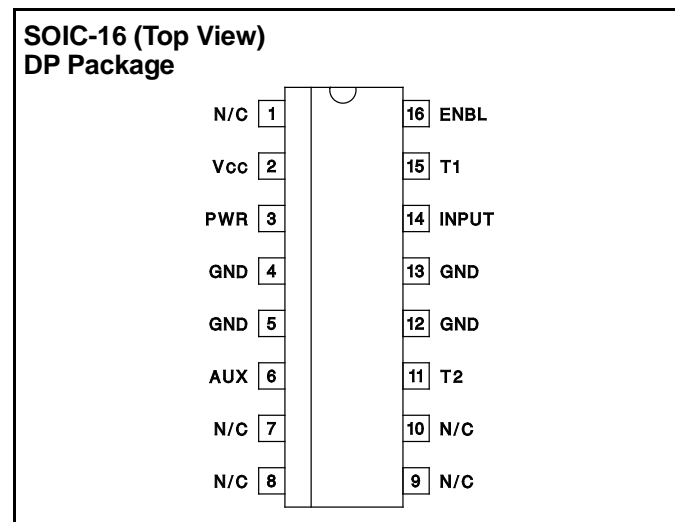
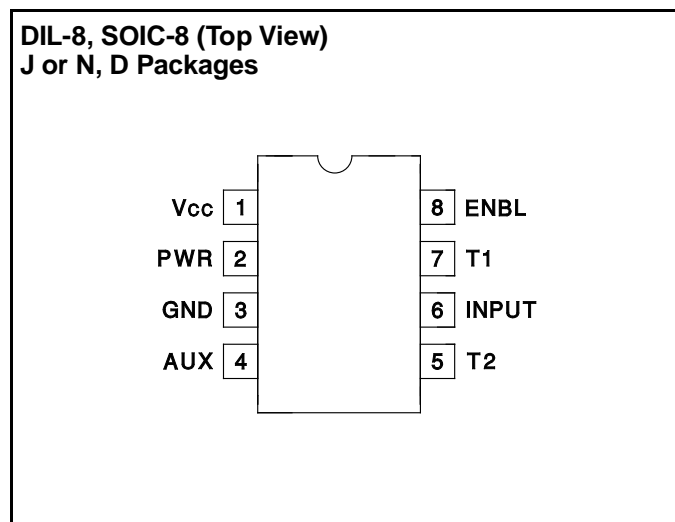
Supply Voltage V_{CC}	20V
Power Driver IOH	
continuous	-200mA
peak	-1A
Power Driver IOL	
continuous	400mA
peak	2A
Auxiliary Driver IOH	
continuous	-100mA
peak	-500mA
Auxiliary Driver IOL	
continuous	200mA
peak	1A

Input Voltage Range (INPUT, ENBL)	-0.3V to 20V
Storage Temperature Range.	-65°C to 150°C
Operating Junction Temperature (Note 1)	150°C
Lead Temperature (Soldering 10 seconds)	300°C

Note 1: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals.

Note 2: Consult Packaging Section of databook for thermal limitations and specifications of packages.

CONNECTION DIAGRAMS



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, $V_{CC} = 15V$, $ENBL \geq 2V$, $R_{T1} = 100k\Omega$ from T1 to GND, $R_{T2} = 100k\Omega$ from T2 to GND, and $-55^\circ C < T_A < 125^\circ C$ for the UC1714/5, $-40^\circ C < T_A < 85^\circ C$ for the UC2714/5, and $0^\circ C < T_A < 70^\circ C$ for the UC3714/5, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Overall					
V_{CC}		7		20	V
I_{CC} , nominal	$ENBL = 2.0V$		18	24	mA
I_{CC} , sleep mode	$ENBL = 0.8V$		200	300	μA
Power Driver (PWR)					
Pre Turn-on PWR Output, Low	$V_{CC} = 0V$, $I_{OUT} = 10mA$, $ENBL \leq 0.8V$		0.3	1.6	V
PWR Output Low, Sat. (V_{PWR})	$INPUT = 0.8V$, $I_{OUT} = 40mA$		0.3	0.8	V
	$INPUT = 0.8V$, $I_{OUT} = 400mA$		2.1	2.8	V
PWR Output High, Sat. ($V_{CC} - V_{PWR}$)	$INPUT = 2.0V$, $I_{OUT} = -20mA$		2.1	3	V
	$INPUT = 2.0V$, $I_{OUT} = -200mA$		2.3	3	V
Rise Time	$C_L = 2200pF$		30	60	ns
Fall Time	$C_L = 2200pF$		25	60	ns
T1 Delay, AUX to PWR	INPUT rising edge, $R_{T1} = 10k\Omega$ (Note 4)	20	35	80	ns
T1 Delay, AUX to PWR	INPUT rising edge, $R_{T1} = 100k\Omega$ (Note 4)	350	500	700	ns
PWR Prop Delay	INPUT falling edge, 50% (Note 3)		35	100	ns
Auxiliary Driver (AUX)					
AUX Output Low, Sat. (V_{AUX})	$V_{IN} = 2.0V$, $I_{OUT} = 20mA$		0.3	0.8	V
	$V_{IN} = 2.0V$, $I_{OUT} = 200mA$		1.8	2.6	V

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated, $V_{CC} = 15V$, $ENBL \geq 2V$, $R_{T1} = 100k\Omega$ from T1 to GND, $R_{T2} = 100k\Omega$ from T2 to GND, and $-55^{\circ}C < T_A < 125^{\circ}C$ for the UC1714/5, $-40^{\circ}C < T_A < 85^{\circ}C$ for the UC2714/5, and $0^{\circ}C < T_A < 70^{\circ}C$ for the UC3714/5, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Auxiliary Driver (AUX) (cont.)					
AUX Output High, Sat ($V_{CC} - V_{AUX}$)	$V_{IN} = 0.8V$, $I_{OUT} = -10mA$		2.1	3.0	V
	$V_{IN} = 0.8V$, $I_{OUT} = -100mA$		2.3	3.0	V
Rise Time	$C_L = 1000pF$		45	60	ns
Fall Time	$C_L = 1000pF$		30	60	ns
T2 Delay, PWR to AUX	INPUT falling edge, $R_{T2} = 10k\Omega$ (Note 4)	20	50	80	ns
T2 Delay, PWR to AUX	INPUT falling edge, $R_{T2} = 100k\Omega$ (Note 4)	250	350	550	ns
AUX Prop Delay	INPUT rising edge, 50% (Note 3)		35	80	ns
Enable (ENBL)					
Input Threshold		0.8	1.2	2.0	V
Input Current, I_{IH}	ENBL = 15V		1	10	μA
Input Current, I_{IL}	ENBL = 0V		-1	-10	μA
T1					
Current Limit	T1 = 0V		-1.6	-2	mA
Nominal Voltage at T1		2.7	3	3.3	V
ZVS Delay	T1 = 2.5V, (Note 5)		40	70	ns
T2					
Current Limit	T2 = 0V		-1.2	-2	mA
Nominal Voltage at T2		2.7	3	3.3	V
ZVS Delay	T2 = 2.5V, (Note 5)		50	100	ns
Input (INPUT)					
Input Threshold		0.8	1.4	2.0	V
Input Current, I_{IH}	INPUT = 15V		1	10	μA
Input Current, I_{IL}	INPUT = 0V		-5	-20	μA

Note 3: Propagation delay times are measured from the 50% point of the input signal to the 10% point of the output signal's transition with no load on outputs.

Note 4: T1 (T2) Delay is defined as the time between the 10% transition point of AUX (PWR) and the 10% transition point of PWR (AUX) with no capacitive load on either output.

Note 5: ZVS Delay is defined as : for the PWR output, the 10% transition point of its rising edge measured from the 50% point of the rising edge of INPUT and for the AUX, the 10% transition point of its rising edge on the UC1715 or the 90% transition point of its falling edge on the UC1714 measured from the 50% point of the falling edge of INPUT.

PIN DESCRIPTIONS

AUX: The AUX switches immediately at INPUT's rising edge but waits through the T2 delay after INPUT's falling edge before switching. AUX is capable of sourcing 0.5A and sinking 1.0A of drive current. See the Time Relationships diagram below for the difference between the UC1714 and UC1715 for INPUT, MAIN, and AUX. During sleep mode, AUX is inactive with a high impedance.

ENBL: The ENBL input switches at TTL logic levels (approximately 1.2V), and its input range is from 0V to 20V. The ENBL input will place the device into sleep mode when it is a logical low. The current into V_{CC} during the sleep mode is typically 220 μA .

GND: This is the reference pin for all input voltages and the return point for all device currents. It carries the full

peak sinking current from the outputs. Any tendency for the outputs to ring below GND voltage must be damped or clamped such that GND remains the most negative potential.

INPUT: The input switches at TTL logic levels (approximately 1.4V) but the allowable range is from 0 to 20V, allowing direct connection to most common IC PWM controller outputs. The rising edge immediately switches the AUX output, and initiates a timing delay, T1, before switching on the PWR output. Similarly, the INPUT falling edge immediately turns off the PWR output and initiates a timing delay, T2, before switching the AUX output.

It should be noted that if the input signal comes from a controller with FET drive capability, this signal provides

PIN DESCRIPTIONS (cont.)

another option. INPUT and PWR provide a delay only at the leading edge while INPUT and AUX provide the delay at the trailing edge.

PWR: The PWR output waits for the T1 delay after the INPUT's rising edge before switching on, but switches off immediately at INPUT's falling edge (neglecting propagation delays). This output is capable of sourcing 1A and sinking 2A of peak gate drive current. PWR output includes a passive, self-biased circuit which holds this pin active low, when $ENBL \leq 0.8V$ regardless of VCC's voltage.

T1: A resistor to ground programs the time delay between AUX switch turn-off and PWR turn-on.

T2: This pin functions in the same way as T1 but controls the time delay between PWR turn-off and activation of the AUX switch.

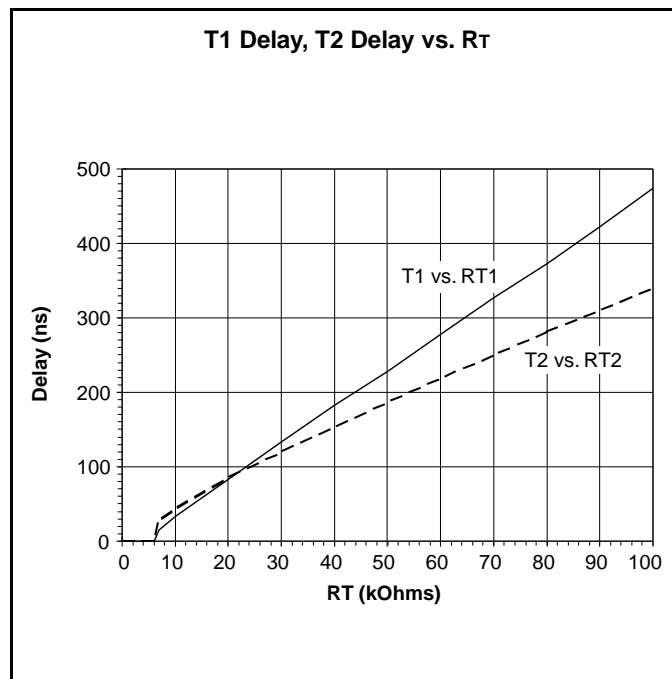
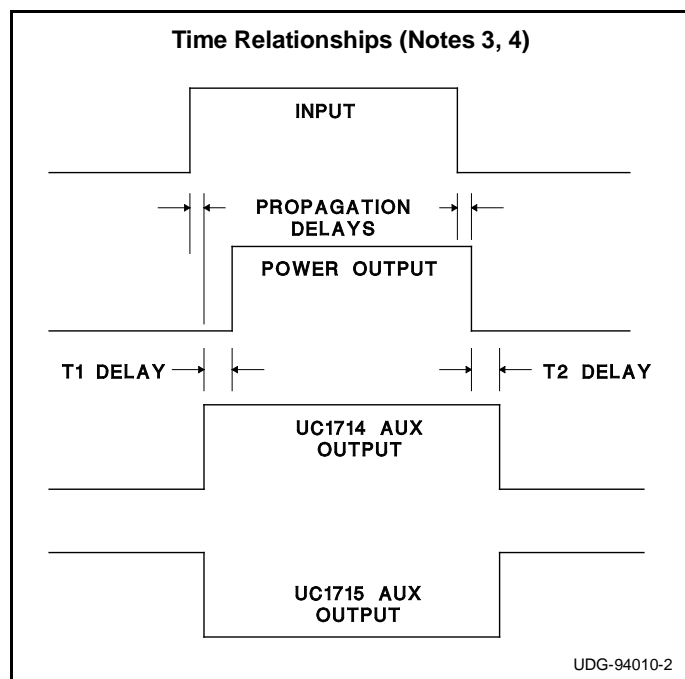
T1, T2: The resistor on each of these pins sets the charg-

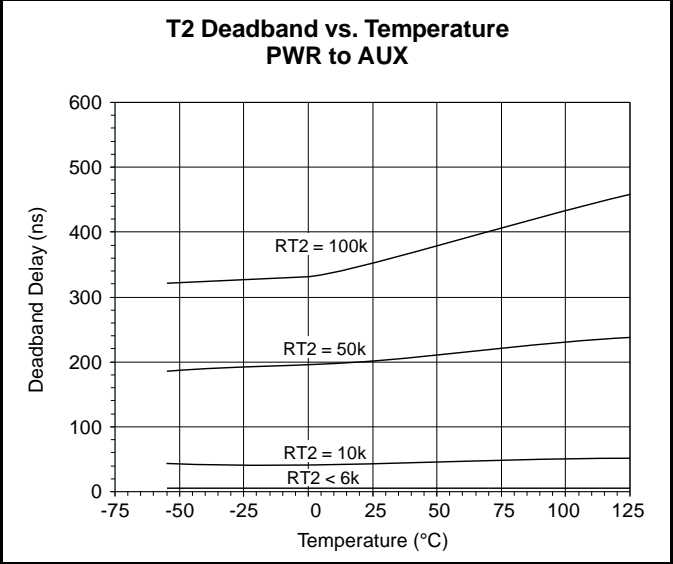
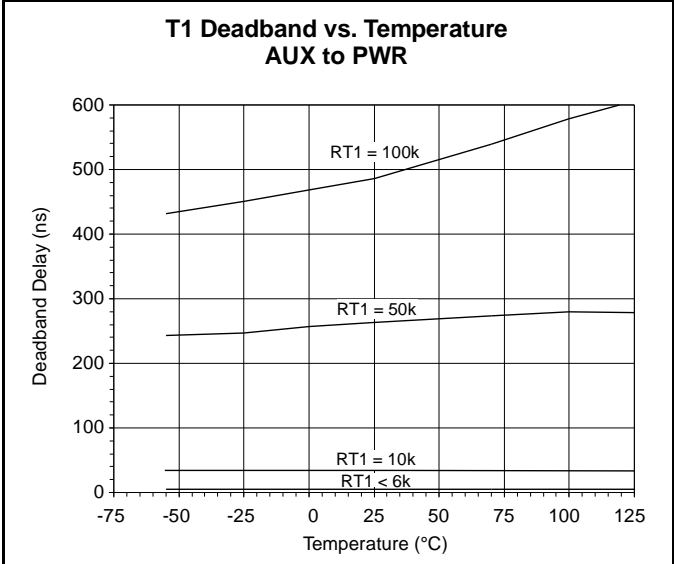
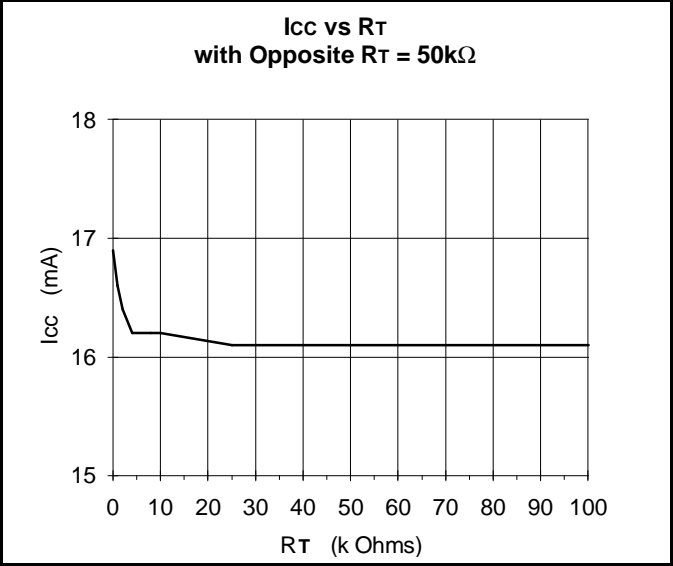
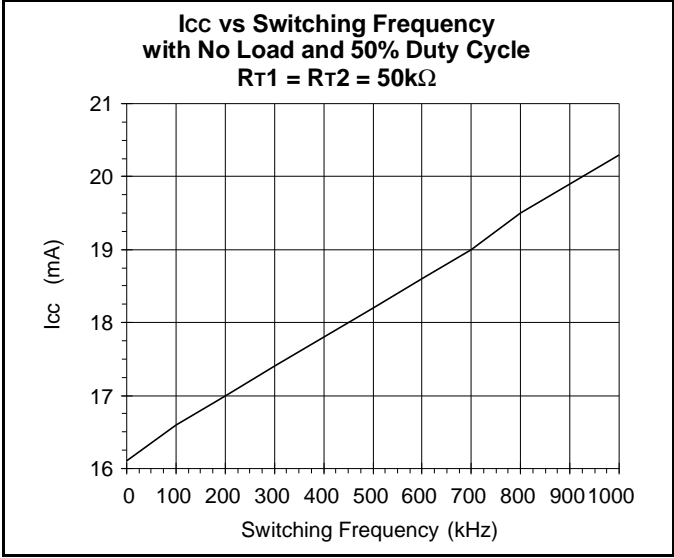
ing current on internal timing capacitors to provide independent time control. The nominal voltage level at each pin is 3V and the current is internally limited to 1mA. The total delay from INPUT to each output includes a propagation delay in addition to the programmable timer but since the propagation delays are approximately equal, the relative time delay between the two outputs can be assumed to be solely a function of the programmed delays. The relationship of the time delay vs. RT is shown in the Typical Characteristics curves.

Either or both pins can alternatively be used for voltage sensing in lieu of delay programming. This is done by pulling the timer pins below their nominal voltage level which immediately activates the timer output.

Vcc: The Vcc input range is from 7V to 20V. This pin should be bypassed with a capacitor to GND consistent with peak load current demands.

TYPICAL CHARACTERISTICS





TYPICAL APPLICATIONS

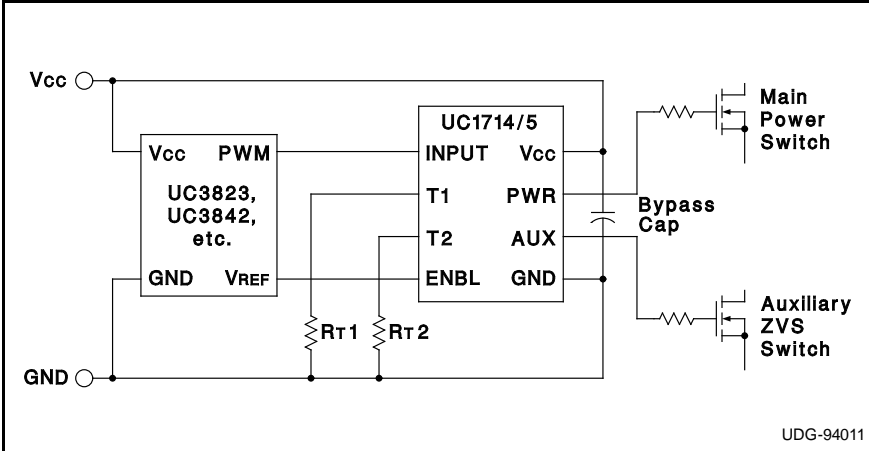


Figure 1. Typical Application With Timed Delays

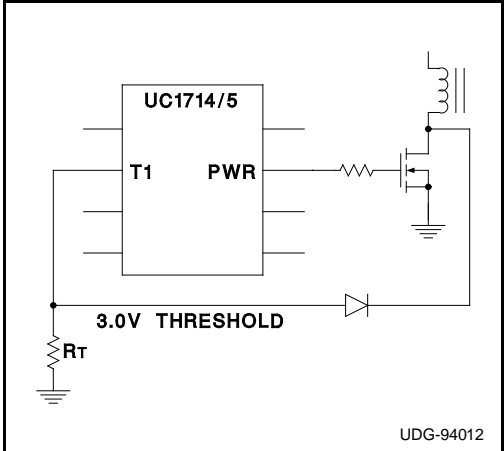
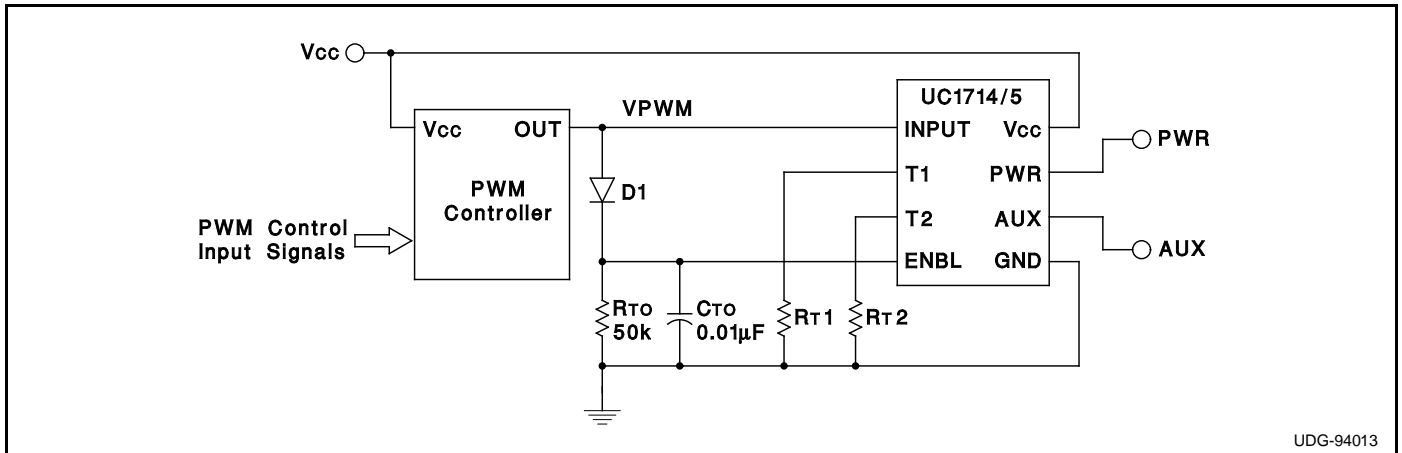


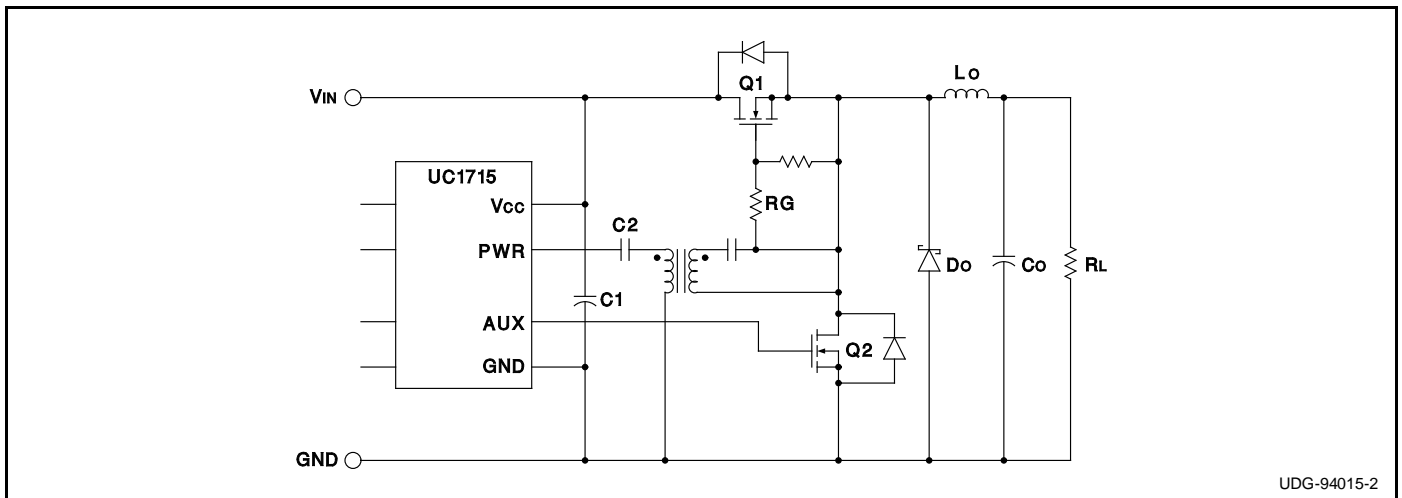
Figure 2. Using the Timer Input for Zero-Voltage Sensing

TYPICAL APPLICATIONS (cont.)



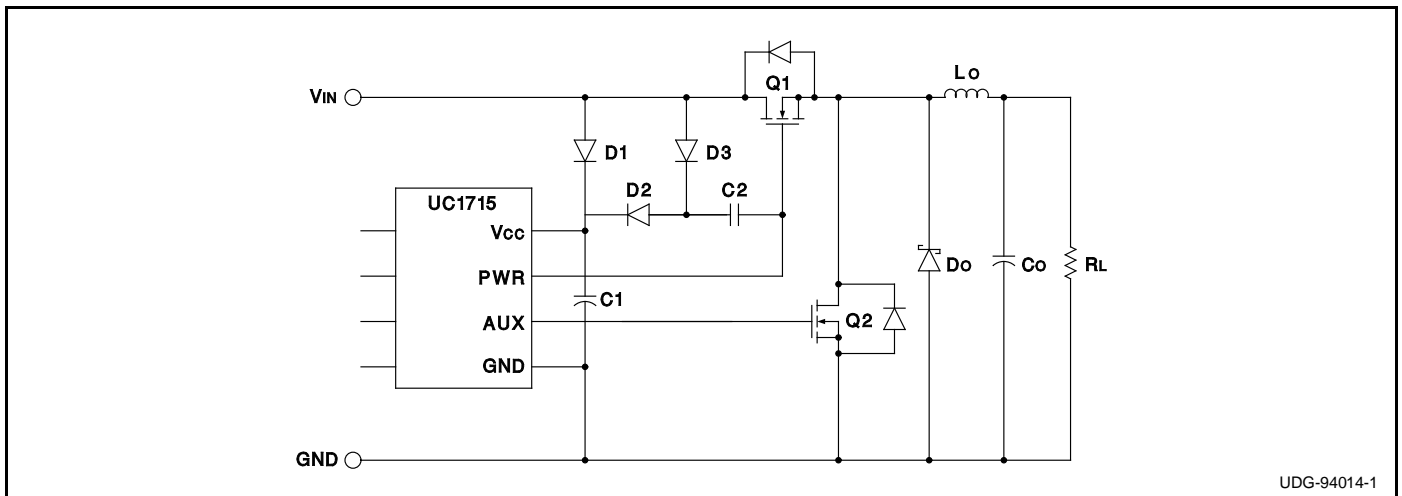
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Figure 3. Self-actuated Sleep Mode with the Absence of an Input PWM Signal. Wake Up Occurs with the First Pulse while Turn-off is Determined by the $R_{T0} \bullet C_{T0}$ Time Constant



UDG-94015-2

Figure 4. Using the UC1715 as a Complementary Synchronous Rectifier Switch Driver with N-Channel FETs



UDG-94014-1

Figure 5. Synchronous Rectifier Application with a Charge Pump to Drive the High-Side N-Channel Buck Switch. V_{IN} is Limited to 10V as V_{CC} will Rise to Approximately $2V_{IN}$.

TYPICAL APPLICATIONS (cont.)

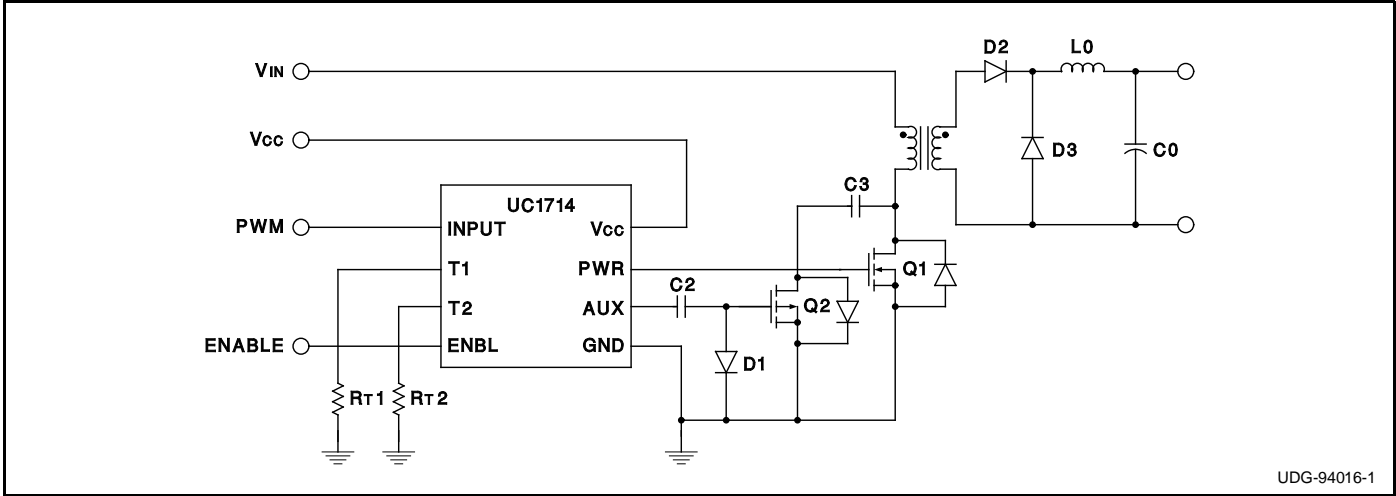


Figure 6. Typical Forward Converter Topology with Active Reset Provided by the UC1714 Driving an N-Channel Switch (Q1) and a P-Channel Auxilliary Switch (Q2)

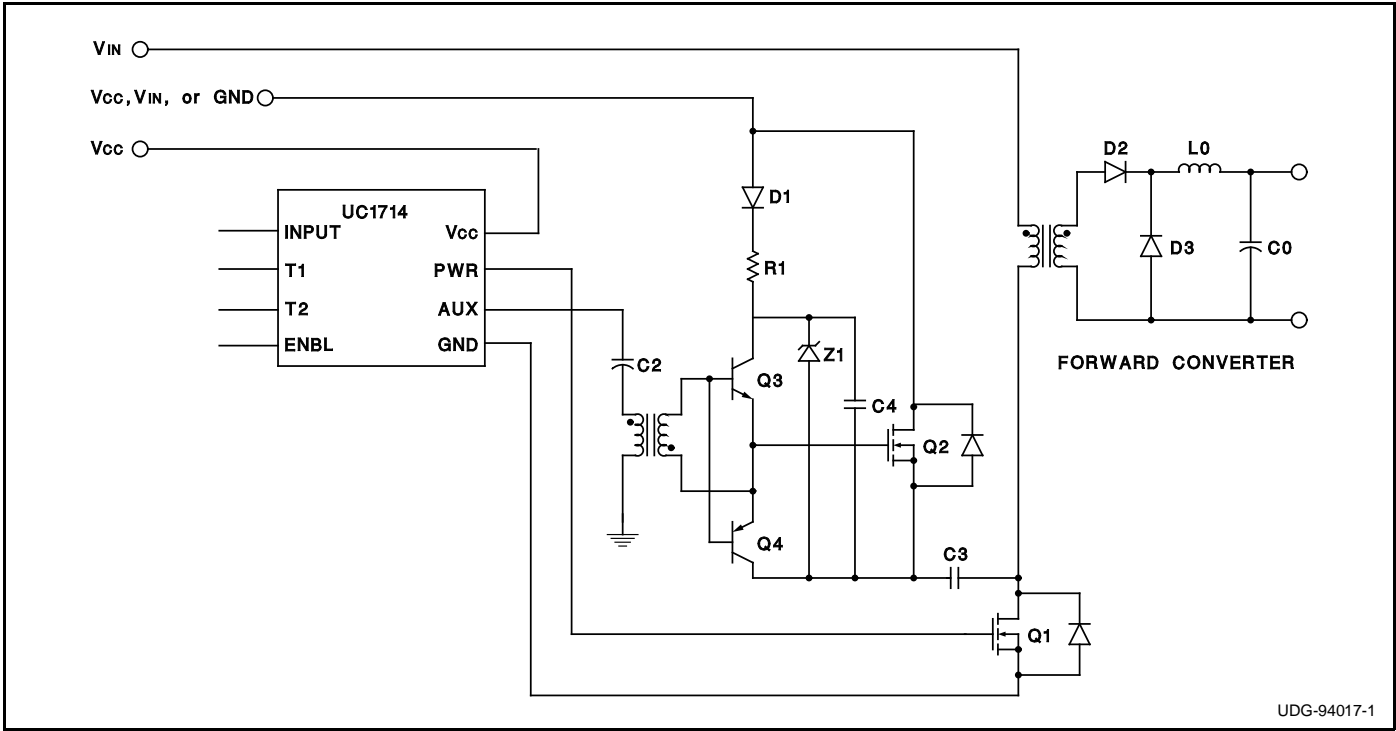


Figure 7. Using an N-Channel Active Reset Switch with a Floating Drive Command